IN THE UNITED STATES DISTRICT COURT
FOR THE WESTERN DISTRICT OF TEXAS
WACO DIVISION

WHIRLWIND LICENSING, LLC	)	
Plaintiff,	)	
	)	**Civil Action No. 6:21-cv-01236**
v.	)	
	)	
CYPRESS SEMICONDUCTOR CORP.	)	**JURY TRIAL DEMANDED**
Defendant.	)	

PLAINTIFF'S ORIGINAL COMPLAINT FOR PATENT INFRINGEMENT

Whirlwind Licensing, LLC ("Whirlwind") files this Original Complaint and demand for jury trial seeking relief from patent infringement of the claims of U.S. Patent No. 8,319,537 ("the '537 patent") (referred to as the "Patent-in-Suit") by Cypress Semiconductor Corp. ("Cypress").

I. THE PARTIES

1. Plaintiff Whirlwind is a Texas Limited Liability Company with its principal place of business located at 3333 Preston Road STE 300 #1051, Frisco, TX 75034.

2. On information and belief, Cypress is a corporation organized and existing under the laws of the state of Delaware, with a place of business located at 5204 E. Ben White Blvd., Austin, TX 78741. On information and belief, Cypress sells and offers to sell products and services throughout Texas, including in this judicial district, and introduces products and services that perform infringing methods or processes into the stream of commerce knowing that they would be sold in Texas and this judicial district. Cypress can be served with process at its registered agent, Corporation Service Company d/b/a CSC-Lawyers Incorporating Service Company 211 E. 7th Street, Suite 620, Austin, TX 78701 or anywhere else it may be found.

II. JURISDICTION AND VENUE

3. This Court has original subject-matter jurisdiction over the entire action pursuant to 28 U.S.C. §§ 1331 and 1338(a) because Plaintiff's claim arises under an Act of Congress relating to patents, namely, 35 U.S.C. § 271.

4. This Court has personal jurisdiction over Defendant because: (i) Defendant is present within or has minimum contacts within the State of Texas and this judicial district; (ii) Defendant has purposefully availed itself of the privileges of conducting business in the State of Texas and in this judicial district; and (iii) Plaintiff's cause of action arises directly from Defendant's business contacts and other activities in the State of Texas and in this judicial district.

5. Venue is proper in this district under 28 U.S.C. §§ 1391(b) and 1400(b). Defendant has committed acts of infringement and has (1) "a physical place in the district;" (2) that is "regular and established;" and (3) is a "the place of the defendant." Further, venue is proper because Defendant conducts substantial business in this forum, directly or through intermediaries, including: (i) at least a portion of the infringements alleged herein; and (ii) regularly doing or soliciting business, engaging in other persistent courses of conduct and/or deriving substantial revenue from goods and services provided to individuals in Texas and this District.

III. INFRINGEMENT

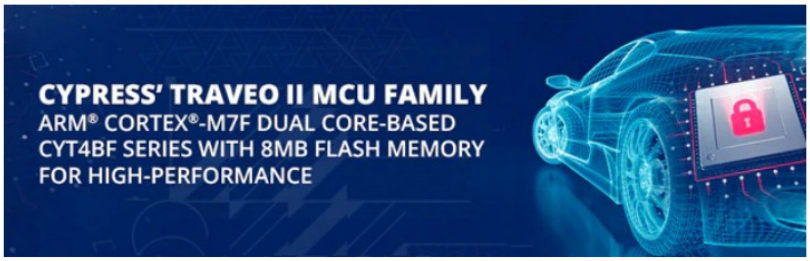
A. Infringement of the '537 Patent

6. On Nov 27, 2012, U.S. Patent No. 8,319,537 ("the '537 patent", included as an attachment and part of this Complaint) entitled "Modulation Profile Generator and Spread Spectrum Clock Generator Including the Same" was duly and legally issued by the U.S. Patent and Trademark Office. Whirlwind owns the '537 patent by assignment.

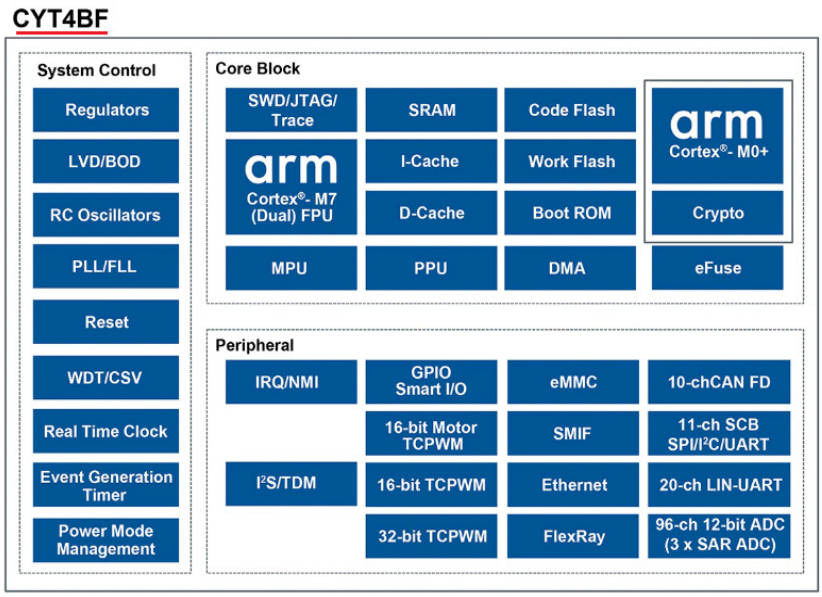
7. The '537 patent provide an apparatus and associated systems and methods for a modulation profile generator and spread spectrum clock generator including the modulation profile generator.

8. Cypress designs, manufactures, markets and sells systems and devices including, but not limited to, the Cypress Traveo II for Body CYT4BF Series system, that infringe one or more claims of the '537 patent, including one or more of claims 1-19, literally or under the doctrine of equivalents. Defendant put the inventions claimed by the '537 Patent into service (i.e., used them); but for Defendant's actions, the claimed-inventions embodiments involving Defendant's products and services would never have been put into service. Defendant's acts complained of herein caused those claimed-invention embodiments as a whole to perform, and Defendant's procurement of monetary and commercial benefit from it.

9. Support for the allegations of infringement may be found in the following preliminary table:

US8319537B2	Cypress Traveo II for Body CYT4BF Series ("The accused product")
17. A modulation profile generating method comprising:	The accused product practices, at least in internal testing and usages, a modulation profile generating method (e.g., generating spread-spectrum clock modulation profile such as triangle, Hershey kiss, etc.). Cypress Traveo™ II for Body CYT4BF Series 

https://www.cypress.com/products/cypress-traveo-ii-body-cyt4bf-series



https://www.cypress.com/products/cypress-traveo-ii-body-cyt4bf-series

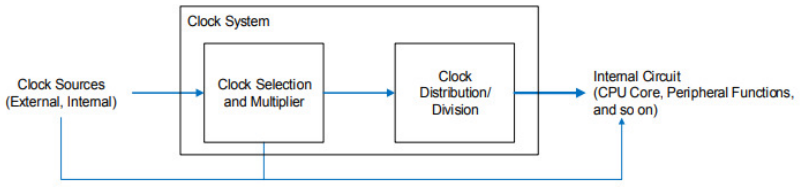
Clock System for Traveo II Family MCUs

Overview of Clock System

The clock system in this series of MCUs are divided into two blocks. One selects the clock resources (such as external oscillation and internal oscillation) and multiplies the clock (using FLL and PLL). The other distributes and divides clocks to the CPU cores, and other peripheral functions. However, there are some exceptions such as RTC that can connect directly to a clock resource.

Figure 1 shows the overview of the Clock System structure.

Figure 1. The Overview of the Clock System Structure



https://www.infineon.com/dgdl/Infineon-Clock_Configuration_Setup_in_Traveo_II_Family_CYT4B_Series-

ApplicationNotes-v01_00-EN.pdf?fileId=5546d462749a7c2d01749b3646a00d08

Explanation of the Clock System Function

This section explains the functions of the clock system.

Figure 2 shows the details of the Clock Selection and Multiplier block. This block generates root frequency clocks CLK_HF0 to CLK_HF7 from the clock resources. This block has the capability to select the one of the supported clock resources, FLL, and PLL to generate the required high-speed clock. This MCU supports two types of PLLs: PLL without SSCG (Spread Spectrum Clock Generation) and Fractional Operation (PLL200#x), and PLL with SSCG and Fractional Operation (PLL400#x).

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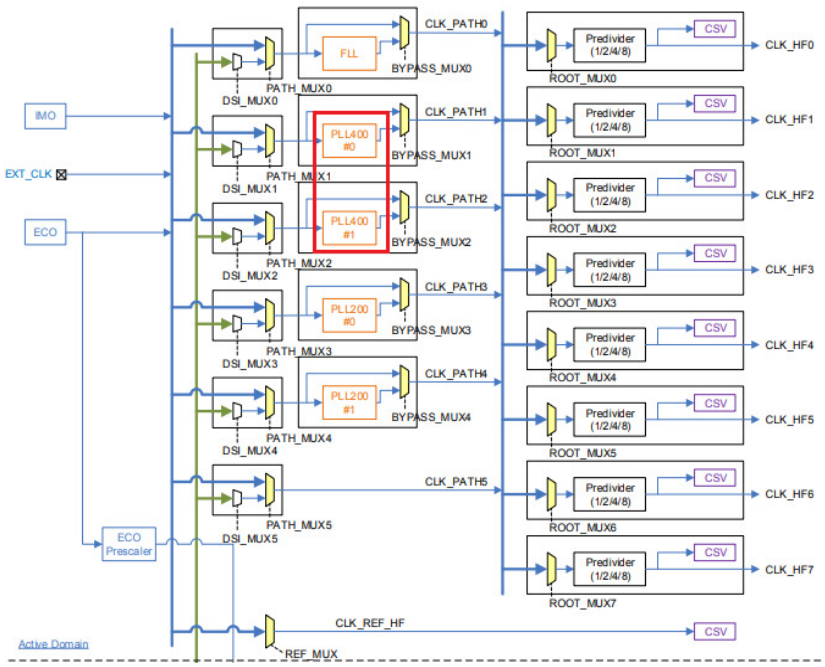
Figure 2. Block Diagram



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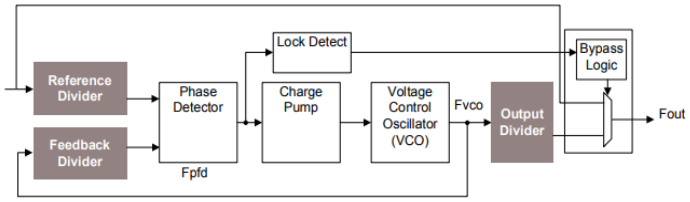
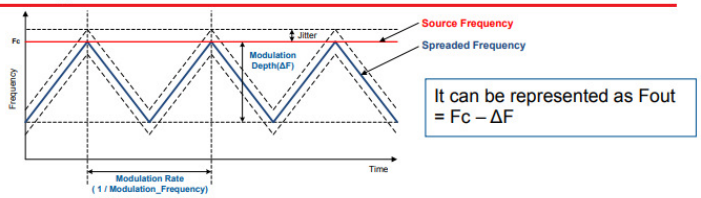
	ApplicationNotes-v01_00-EN.pdf?fileId=5546d462749a7c2d01749b3646a00d08 PLL — Generates high-frequency clock. There are two kinds of PLL: PLL200 and PLL400. PLL200 is without SSCG and Fractional Operation and PLL400 is with SSCG and Fractional Operation. BYPASS_MUX — Selects the clock to be output to CLK_PATH. In case of FLL, the clock that can be selected is either FLL output or clock input to FLL. https://www.infineon.com/dgdl/Infineon-Clock_Configuration_Setup_in_Traveo_II_Family_CYT4B_Series-ApplicationNotes-v01_00-EN.pdf?fileId=5546d462749a7c2d01749b3646a00d08 › PLL configuration parameters (CYT4BF)[1] https://www.infineon.com/dgdl/Infineon-Traveo_II_Body_High_and_Cluster-2D_Clock_System-Training-v01_00-EN.pdf?fileId=5546d46277921c320177a26116713407

Parameters	PLL w/o SSCG and Fractional Operation	PLL with SSCG and Fractional Operation
Fref	3.988 to 33.34 MHz	3.988 to 33.34 MHz
Fout (Fvco/Output divider)	11 to 200 MHz	25 to 350 MHz
Fpfd (Fref/Reference divider)	4 to 8 MHz	8 to 20 MHz
Fvco (Fpfd * Feedback divider)	170 to 400 MHz	400 to 800 MHz



Configuration for SSCG

- Spread energy contained in the narrow band of the clock source to a wide band



- The parameters on the PLL configuration[1] are as follows:
  - Modulation Depth: Between -3%, -2%, -1%, or - 0.5%
  - Modulation Rate: Between Fpfd/4096, Fpfd/2048, Fpfd/1024, or Fpfd/512
  - Modulation Type: Down-spread mode only

Advantage

- Reduces the peak spectral amplitude of the fundamental and the harmonics to lower radiated emission from the clock source

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Upon information and belief, while generating spread-spectrum clock signal using the accused product, a clock signal having clock spectrum flatter, “Hershey Kiss”, is generated as a modulation waveform.

An almost flat spectrum can be obtained by with more EMI reduction using a Hershey kiss (Lexmark) spread profile (see Figure 5b). The Hershey kiss spread profile has a radically distinctive shape where the clock frequency sweeps at a higher rate near the start and end frequency points and is slowed down at the center. Because of the higher rate of frequency change near the two boundary points, the two side lobes are attenuated and the reduced energy is distributed over the center flat portion of the spectrum. This results in a dramatic change by approximately flattening the complete energy spectrum. As shown in figure, the Hershey kiss spread profile has provided a further 1.13dB reduction. This reduction can be higher based on the actual frequency values.

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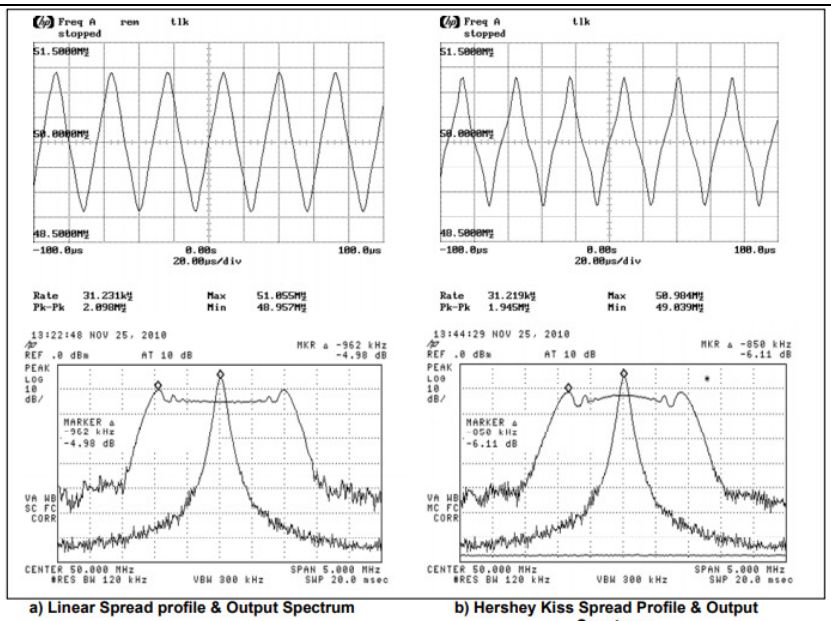
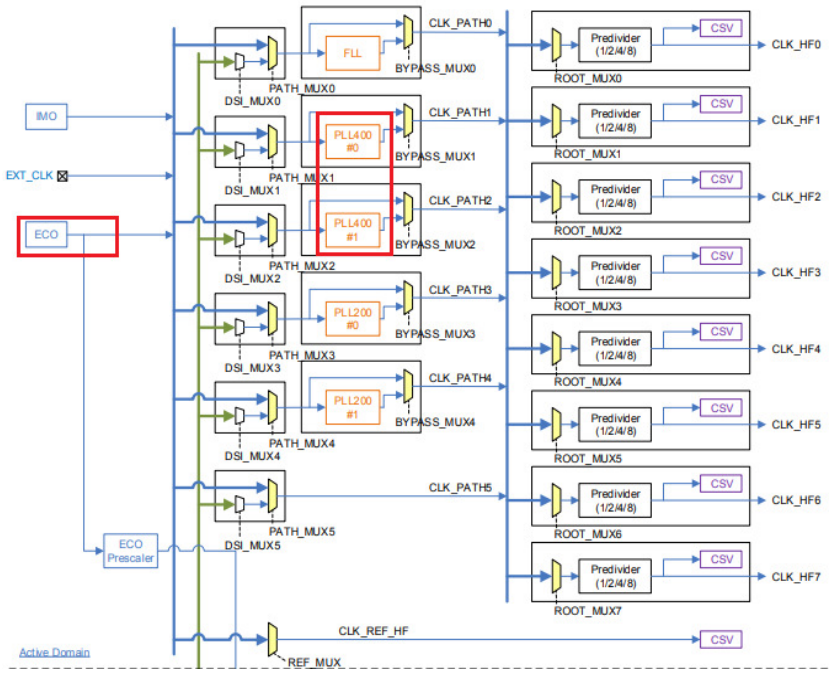
	 a) Linear Spread profile & Output Spectrum b) Hershey Kiss Spread Profile & Output Spectrum https://www.cypress.com/file/106246/download
generating an input signal having a predetermined frequency and waveform;	The accused product practices generating an input signal (e.g., ECO clock signal) having a predetermined frequency (e.g., ECO signal frequency) and waveform (e.g., ECO signal waveform).

Figure 2. Block Diagram



https://www.infineon.com/dgdl/Infineon-Clock_Configuration_Setup_in_Traveo_II_Family_CYT4B_Series-ApplicationNotes-v01_00-EN.pdf?fileId=5546d462749a7c2d01749b3646a00d08

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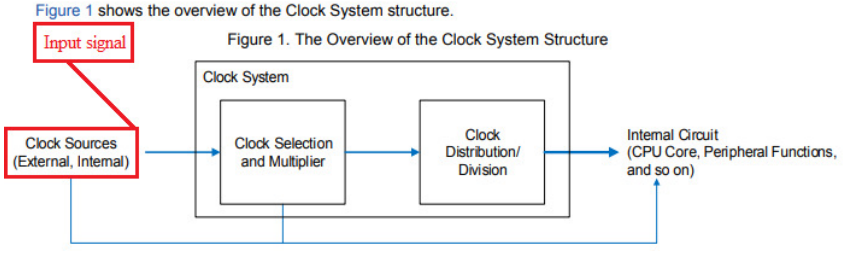
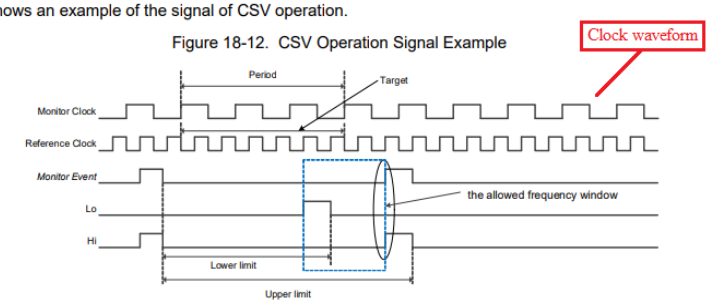


https://www.infineon.com/dgdl/Infineon-Clock_Configuration_Setup_in_Traveo_II_Family_CYT4B_Series-

	ApplicationNotes-v01_00-EN.pdf?fileId=5546d462749a7c2d01749b3646a00d08 | Terms	Description | |---|---| | IMO | Internal Main Oscillator | | ILO | Internal Low-speed Oscillators | | ECO | External Crystal Oscillator | | WCO | Watch Crystal Oscillator | https://www.infineon.com/dgdl/Infineon-Clock_Configuration_Setup_in_Traveo_II_Family_CYT4B_Series-ApplicationNotes-v01_00-EN.pdf?fileId=5546d462749a7c2d01749b3646a00d08 **Clock Resources** The MCU supports two types of resource inputs: internal and external. Each of these internally supports three types of clocks respectively. ■ Internal clock sources (All of these clocks are enabled by default.): ▫ Internal Main Oscillator (IMO): This is a built-in clock with a frequency of 8 MHz (TYP). ▫ Internal Low-speed Oscillator 0 (ILO0): This is a built-in clock with a frequency of 32 kHz (TYP). ▫ Internal Low-speed Oscillator 1 (ILO1): This clock has the same function as ILO0, but ILO1 can monitor the clock of ILO0. ■ External clock sources (All of these clocks are disabled by default.): ▫ External Crystal Oscillator (ECO): This clock uses an external oscillator whose input frequency range is in between 3.988 and 33.34 MHz. ▫ Watch Crystal Oscillator (WCO): This also uses an external oscillator whose frequency is stable 32.768 kHz, mainly used by the RTC module. ▫ External Clock (EXT_CLK): The EXT_CLK is a 0.25 MHz to 100 MHz range clock that can be sourced from a signal on a designed I/O pin. This clock can be used as the source clock for either PLL or FLL, or can be used directly by the high-frequency clocks. https://www.infineon.com/dgdl/Infineon-Clock_Configuration_Setup_in_Traveo_II_Family_CYT4B_Series-ApplicationNotes-v01_00-EN.pdf?fileId=5546d462749a7c2d01749b3646a00d08 A clock input signal waveform of the accused product is shown.

	Figure 18-12 shows an example of the signal of CSV operation.  https://www.cypress.com/file/513511/download
outputting a function calculation result in the form of a square root graph by using the input signal as an input of a function; and	The accused product practices outputting a function calculation result (e.g., ECO configuration) in the form of a square root graph by using the input signal (e.g., ECO clock signal) as an input of a function (e.g., ECO trimming). As shown below, the accused product provides utilization of PLL400 with ECO. To configure PLL400 with ECO, ECO needs to be configured. It needs to be trimmed (e.g., ECO trimming function). For ECO trimming, a maximum peak oscillation voltage across the crystal, Vp, is calculated using ECO clock signal (e.g., input signal) values as an input for a square root function. Based on the maximum peak oscillation voltage across the crystal Vp, transconductance gm, capacitance and Frequency, ECO is configured (e.g., a function calculation result). The ECO clock signal (e.g., input signal) values are used to calculate Vp, which takes ECO signal values as an input for square root function, based on which trimming values are determined for a configured ECO signal.

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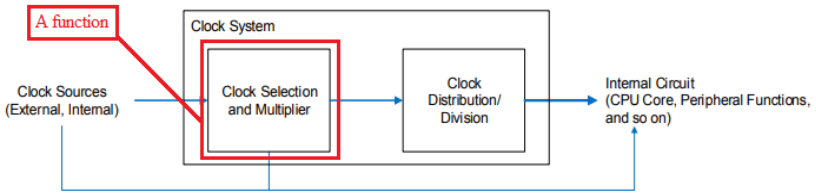

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Figure 2 shows the details of the Clock Selection and Multiplier block. This block generates root frequency clocks CLK_HF0 to CLK_HF7 from the clock resources. This block has the capability to select the one of the supported clock resources, FLL, and PLL to generate the required high-speed clock. This MCU supports two types of PLLs: PLL without SSCG (Spread Spectrum Clock Generation) and Fractional Operation (PLL200#x), and PLL with SSCG and Fractional Operation (PLL400#x).

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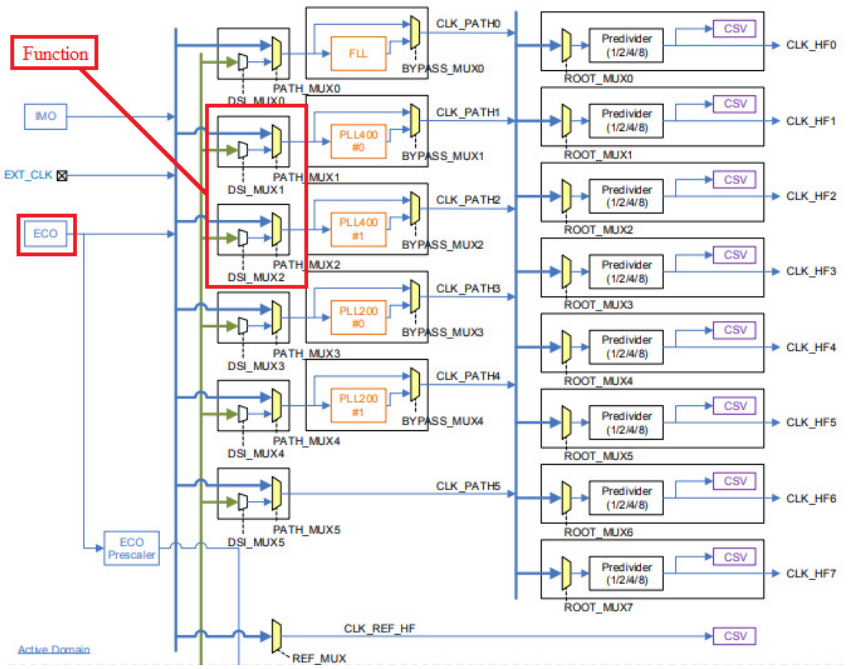

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Terms	Description
IMO	Internal Main Oscillator
ILO	Internal Low-speed Oscillators
ECO	External Crystal Oscillator
WCO	Watch Crystal Oscillator

https://www.infineon.com/dgdl/Infineon-Clock_Configuration_Setup_in_Traveo_II_Family_CYT4B_Series-ApplicationNotes-v01_00-EN.pdf?fileId=5546d462749a7c2d01749b3646a00d08

External clock sources (All of these clocks are disabled by default.):

- External Crystal Oscillator (ECO): This clock uses an external oscillator whose input frequency range is in between 3.988 and 33.34 MHz.
- Watch Crystal Oscillator (WCO): This also uses an external oscillator whose frequency is stable 32.768 kHz, mainly used by the RTC module.

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Table 5. Configuring of PLL Using ECO

Step	Description	Operation	Reference Section
1	Configure ECO	Enable ECO	3.1 Configuring the ECO
2	Configure PATH_MUX	Select ECO	5.1 Configuring the CLK_PATHx
3	Configure PLL400#0	To configure the PLL output as 350 MHz: FEEDBACK_DIV = 175 REFERENCE_DIV = 1 OUTPUT_DIV = 2	4.2 Configuring the PLL
4	Configure PLL400#1	To configure the PLL output as 196.608 MHz: FEEDBACK_DIV = 196 REFERENCE_DIV = 1 OUTPUT_DIV = 4 LOCK_DELAY = 1 FRAC_DIV = 10200547	
5	Configure PLL200#0	To configure the PLL output as 200 MHz: FEEDBACK_DIV = 100 REFERENCE_DIV = 1 OUTPUT_DIV = 4	
6	Configure PLL200#1	To configure the PLL output as 80 MHz: FEEDBACK_DIV = 100 REFERENCE_DIV = 1 OUTPUT_DIV = 5	
7	Configure CLK_HF	CLK_HF0: CLK_ROOT_SELECT0. ROOT_MUX=3 CLK_HF1: CLK_ROOT_SELECT1. ROOT_MUX=1 CLK_HF2: CLK_ROOT_SELECT2. ROOT_MUX=4 CLK_HF3: CLK_ROOT_SELECT3. ROOT_MUX=1 CLK_HF4: CLK_ROOT_SELECT4. ROOT_MUX=3 CLK_HF5: CLK_ROOT_SELECT5. ROOT_MUX=2 CLK_HF6: CLK_ROOT_SELECT6. ROOT_MUX=3	5.2 Configuring the CLK_HFx
8	Configure CLK_FAST_0 and CLK_FAST_0	INT_DIV = 0	5.4 Configuring the CLK_FAST_0/CLK_FAST_1
9	Configure CLK_MEM	INT_DIV = 1	5.5 Configuring the CLK_MEM
9	Configure CLK_SLOW	INT_DIV = 0	5.7 Configuring the CLK_SLOW
10	Configure CLK_PERI	INT_DIV = 1	5.6 Configuring the CLK_PERI
11	Configure PCLK	Set according to peripheral function to be used	5.9 Configuring the PCLK

https://www.infineon.com/dgdl/Infineon-Clock_Configuration_Setup_in_Traveo_II_Family_CYT4B_Series-ApplicationNotes-v01_00-EN.pdf?fileId=5546d462749a7c2d01749b3646a00d08

Configuring the ECO

By default, the ECO is disabled and needs to be enabled for usage. Also, trimming is necessary to use ECO. See the Architecture TRM for more information. Figure 9 shows how to configure the clock for trimming of ECO, and Figure 10 shows how to configure registers for enabling the ECO.

To disable the ECO, write '0' to the ECO_EN bit of the CLK_ECO_CONFIG register.

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18.2.2.1 ECO Trimming

The ECO supports a wide variety of crystals and ceramic resonators with the nominal frequency range specification described in the datasheet. The crystal manufacturer typically provides numerical values for parameters, namely the maximum drive level (D_L), the equivalent series resistance (ESR), the ideal shunt capacitance (C_0) and the parallel load capacitance (C_L). These parameters can be used to calculate the transconductance (g_m) and the maximum peak oscillation voltage across the crystal (V_P).

The formula of V_P is as follows. ECO does not support V_P less than 0.3 V.

$$\text{Max peak value: } Vp = \frac{\sqrt{\frac{D_L}{2ESR}}}{\pi f(C_0 + C_L)}$$

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	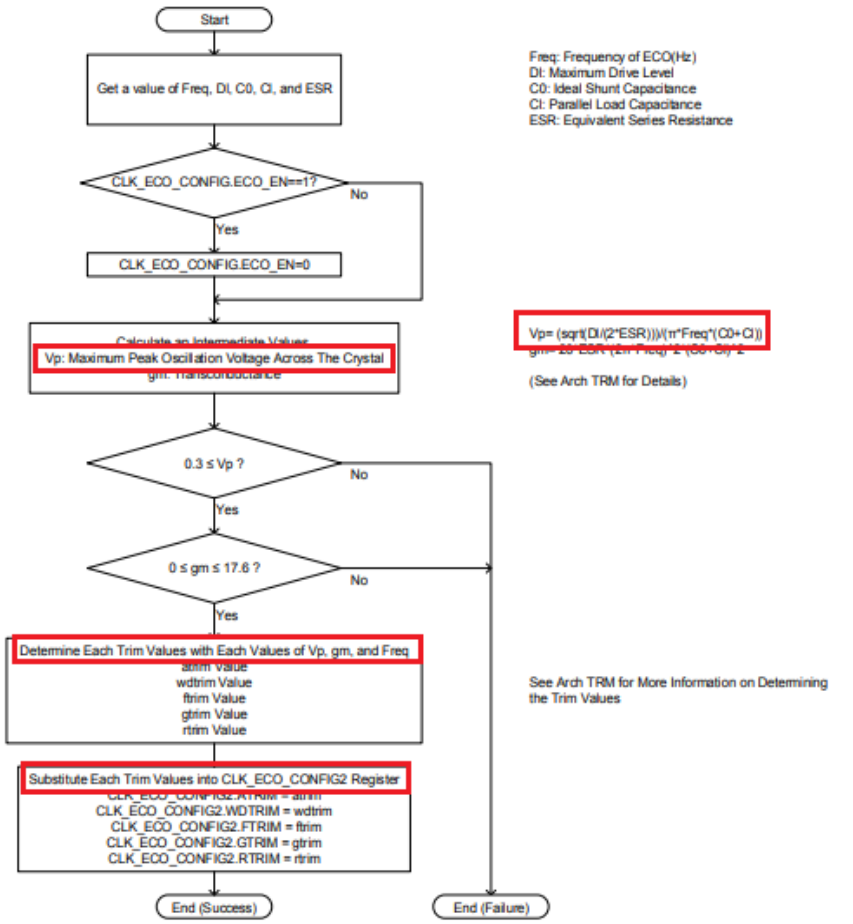 https://www.infineon.com/dgdl/Infineon-Clock_Configuration_Setup_in_Traveo_II_Family_CYT4B_Series-ApplicationNotes-v01_00-EN.pdf?fileId=5546d462749a7c2d01749b3646a00d08
generating a non-linear modulation profile based on the function calculation result.	The accused product, at least in internal testing and usages, practices generating a non-linear modulation profile (e.g., Hershey Kiss modulation profile) based on the function calculation result (e.g., ECO configuration). As shown below, the accused product receives ECO as a clock input signal. The ECO clock input signal requires ECO trimming (e.g., function) before utilizing it for PLL. The configured ECO signal

(e.g., function calculation result) is supplied to PLL. The accused product provides two-type of PLLs, one of that supports spread spectrum clock generation. The accused product provides a SSCG signal by modulating the configured ECO clock signal with a waveform.

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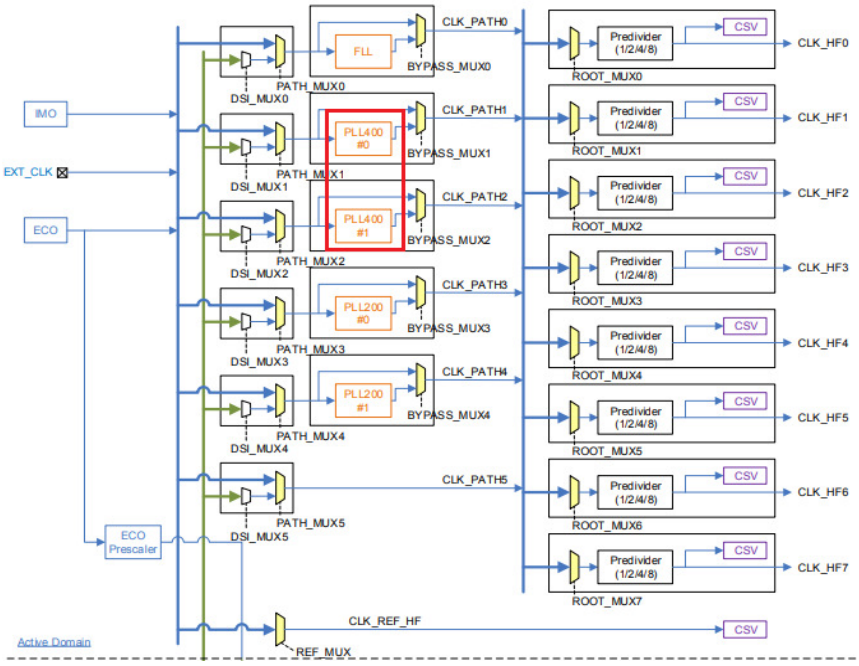
Figure 2. Block Diagram



	https://www.infineon.com/dgdl/Infineon-Clock_Configuration_Setup_in_Traveo_II_Family_CYT4B_Series-ApplicationNotes-v01_00-EN.pdf?fileId=5546d462749a7c2d01749b3646a00d08 **Setting the ECO** The ECO is disabled by default and needs to be enabled for usage. Also, trimming is necessary to use the ECO. This device can set the trimming parameters that control the oscillator according to Crystal Unit and Ceramic Resonator. The method to determine the parameters differs between Crystal Unit and Ceramic Resonator. See the "Setting ECO Parameters" section in the Traveo II User Guide for more information. https://www.infineon.com/dgdl/Infineon-Clock_Configuration_Setup_in_Traveo_II_Family_CYT4B_Series-ApplicationNotes-v01_00-EN.pdf?fileId=5546d462749a7c2d01749b3646a00d08 **Example 1: PLL200 and PLL400 Using ECO** This example demonstrates how to configure PLL with ECO as the clock source. Table 5 lists the procedure. The following are the parameters of PLL using ECO: ■ Clock source: ECO 4 MHz ■ PLL400#0: 350 MHz ■ PLL400#1: 196.608 MHz ■ PLL200#0: 200 MHz ■ PLL200#1: 80 MHz ■ CM7_0/CM7_1 operation clock: 350 MHz ■ CM0+ operation clock: 100 MHz ■ CLK_PERI: 100 MHz ■ CLL_SLOW: 100 MHz https://www.infineon.com/dgdl/Infineon-Clock_Configuration_Setup_in_Traveo_II_Family_CYT4B_Series-ApplicationNotes-v01_00-EN.pdf?fileId=5546d462749a7c2d01749b3646a00d08

Table 5. Configuring of PLL Using ECO

Step	Description	Operation	Reference Section
1	Configure ECO	Enable ECO	3.1 Configuring the ECO
2	Configure PATH_MUX	Select ECO	5.1 Configuring the CLK_PATHx
3	Configure PLL400#0	To configure the PLL output as 350 MHz: FEEDBACK_DIV = 175 REFERENCE_DIV = 1 OUTPUT_DIV = 2	4.2 Configuring the PLL
4	Configure PLL400#1	To configure the PLL output as 196.608 MHz: FEEDBACK_DIV = 196 REFERENCE_DIV = 1 OUTPUT_DIV = 4 LOCK_DELAY = 1 FRAC_DIV = 10200547	
5	Configure PLL200#0	To configure the PLL output as 200 MHz: FEEDBACK_DIV = 100 REFERENCE_DIV = 1 OUTPUT_DIV = 4	
6	Configure PLL200#1	To configure the PLL output as 80 MHz: FEEDBACK_DIV = 100 REFERENCE_DIV = 1 OUTPUT_DIV = 5	
7	Configure CLK_HF	CLK_HF0: CLK_ROOT_SELECT0. ROOT_MUX=3 CLK_HF1: CLK_ROOT_SELECT1. ROOT_MUX=1 CLK_HF2: CLK_ROOT_SELECT2. ROOT_MUX=4 CLK_HF3: CLK_ROOT_SELECT3. ROOT_MUX=1 CLK_HF4: CLK_ROOT_SELECT4. ROOT_MUX=3 CLK_HF5: CLK_ROOT_SELECT5. ROOT_MUX=2 CLK_HF6: CLK_ROOT_SELECT6. ROOT_MUX=3	5.2 Configuring the CLK_HFx
8	Configure CLK_FAST_0 and CLK_FAST_0	INT_DIV = 0	5.4 Configuring the CLK_FAST_0/CLK_FAST_1
9	Configure CLK_MEM	INT_DIV = 1	5.5 Configuring the CLK_MEM
9	Configure CLK_SLOW	INT_DIV = 0	5.7 Configuring the CLK_SLOW
10	Configure CLK_PERI	INT_DIV = 1	5.6 Configuring the CLK_PERI
11	Configure PCLK	Set according to peripheral function to be used	5.9 Configuring the PCLK

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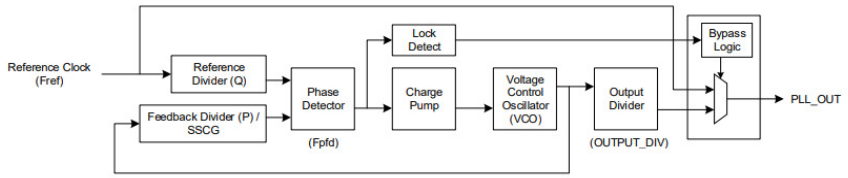
PLL	Generates high-frequency clock. There are two kinds of PLL: PLL200 and PLL400. PLL200 is without SSCG and Fractional Operation and PLL400 is with SSCG and Fractional Operation.
BYPASS_MUX	Selects the clock to be output to CLK_PATH. In case of FLL, the clock that can be selected is either FLL output or clock input to FLL.

https://www.infineon.com/dgdl/Infineon-Clock_Configuration_Setup_in_Traveo_II_Family_CYT4B_Series-ApplicationNotes-v01_00-EN.pdf?fileId=5546d462749a7c2d01749b3646a00d08

18.3.2 PLL with SSCG and Fractional Operation (400-MHz PLL)

See the datasheet to identify where this PLL type is used. See the device-specific datasheet to check whether this PLL is present. The datasheet also specifies the frequency range that can be input to the PLL and the frequency range that the PLL can output. This makes it possible to use the IMO or another clock to generate much higher clock frequencies for the rest of the system. Figure 18-3 shows the block diagram of a PLL with SSCG and fractional operation. This type of PLL is configured in the CLK_PLL400Mx_CONFIG register and the status is confirmed in the CLK_PLL400Mx_STATUS register.

Figure 18-3. PLL with SSCG and Fractional Operation



18.3.2.1 Spread Spectrum Clock Generation (SSCG)

Spread spectrum clock generation (SSCG) is a method by which the energy contained in the narrow band of a clock source is spread over a wider band in a controlled manner, thus reducing the peak spectral amplitude of the fundamental and the harmonics to lower the radiated emission from the clock source. This is achieved by modulating the clock frequency with a waveform. The configuration of the SSCG uses the CLK_PLL400Mx_CONFIG3 register.

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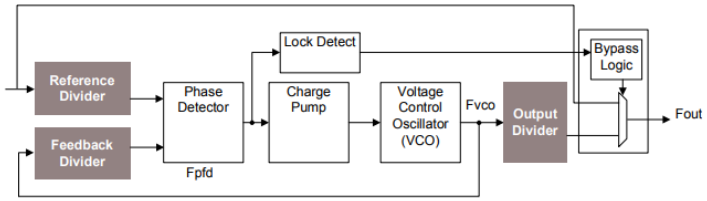
› PLL configuration parameters (CYT4BF)[1]

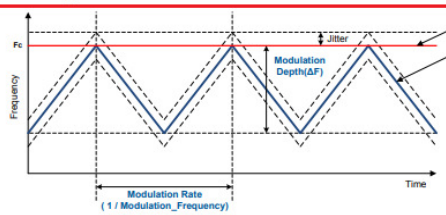
Parameters	PLL w/o SSCG and Fractional Operation	PLL with SSCG and Fractional Operation
Fref	3.988 to 33.34 MHz	3.988 to 33.34 MHz
Fout (Fvco/Output divider)	11 to 200 MHz	25 to 350 MHz
Fpfd (Fref/Reference divider)	4 to 8 MHz	8 to 20 MHz
Fvco (Fpfd * Feedback divider)	170 to 400 MHz	400 to 800 MHz



https://www.infineon.com/dgdl/Infineon-Traveo_II_Body_High_and_Cluster-2D_Clock_System-Training-v01_00-EN.pdf?fileId=5546d46277921c320177a26116713407

Configuration for SSCG

- Spread energy contained in the narrow band of the clock source to a wide band



It can be represented as Fout = Fc – ΔF

- The parameters on the PLL configuration[1] are as follows:
  - Modulation Depth: Between -3%, -2%, -1%, or - 0.5%
  - Modulation Rate: Between Fpfd/4096, Fpfd/2048, Fpfd/1024, or Fpfd/512
  - Modulation Type: Down-spread mode only

Advantage

- Reduces the peak spectral amplitude of the fundamental and the harmonics to lower radiated emission from the clock source

https://www.infineon.com/dgdl/Infineon-Traveo_II_Body_High_and_Cluster-2D_Clock_System-Training-v01_00-EN.pdf?fileId=5546d46277921c320177a26116713407

The accused product provides a SSCG signal by modulating the configured ECO clock signal with a waveform. Upon information and belief, while generating spread-spectrum clock signal using the accused product, an output clock signal having clock spectrum flatter, “Hershey Kiss”, is also generated as a modulated SSCG waveform.

Selection of the spread profile also plays a vital in determining the amount of reduction in peak energy content with SS technique. The spread profile is nothing but the envelope of the frequency variation of modulated signal (spread clock) with

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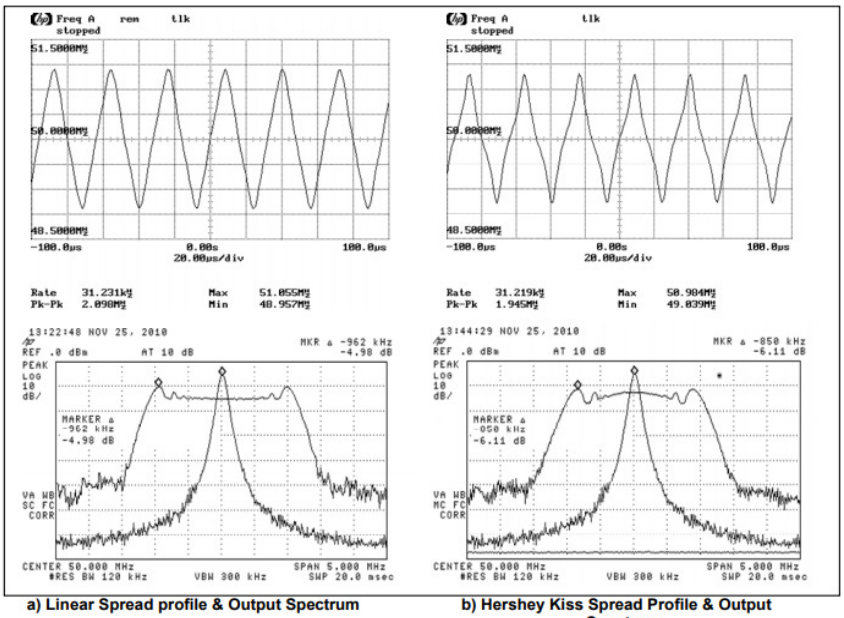
An almost flat spectrum can be obtained by with more EMI reduction using a Hershey kiss (Lexmark) spread profile (see Figure 5b). The Hershey kiss spread profile has a radically distinctive shape where the clock frequency sweeps at a higher rate near the start and end frequency points and is slowed down at the center. Because of the higher rate of frequency change near the two boundary points, the two side lobes are attenuated and the reduced energy is distributed over the center flat portion of the spectrum. This results in a dramatic change by approximately flattening the complete energy spectrum. As shown in figure, the Hershey kiss spread profile has provided a further 1.13dB reduction. This reduction can be higher based on the actual frequency values.

	https://www.cypress.com/file/106246/download  a) Linear Spread profile & Output Spectrum b) Hershey Kiss Spread Profile & Output Spectrum https://www.cypress.com/file/106246/download

10. These allegations of infringement are preliminary and are therefore subject to change. For instance, there are other of Defendant's products that infringe.

11. Cypress has and continues to induce infringement. Cypress has actively encouraged or instructed others (e.g., its customers and/or the customers of its related companies), and continues to do so, on how to use its products and services (e.g., modulation generator products/devices) such as to cause infringement of one or more of claims 1–19 of the '537 patent, literally or under the doctrine of equivalents. Moreover, Cypress has known of the '537 patent and the technology underlying it from at least the date of issuance of the patent or the date of the filing of this lawsuit.

12. Cypress has and continues to contributorily infringe. Cypress has actively encouraged or instructed others (e.g., its customers and/or the customers of its related companies), and continues to do so, on how to use its products and services (e.g., modulation generator products/devices) such as to cause infringement of one or more of claims 1–19 of the '537 patent, literally or under the doctrine of equivalents. Moreover, Cypress has known of the '537 patent and the technology underlying it from at least the date of issuance of the patent or the date of the filing of this lawsuit.

13. Cypress has caused and will continue to cause Whirlwind damage by direct and indirect infringement of (including inducing infringement of) the claims of the '537 patent.

IV. JURY DEMAND

Whirlwind hereby requests a trial by jury on issues so triable by right.

V. PRAYER FOR RELIEF

WHEREFORE, Whirlwind prays for relief as follows:

a. enter judgment that Defendant has infringed the claims of the '537 patent;

b. award Whirlwind damages in an amount sufficient to compensate it for Defendant's infringement of the '537 patent in an amount no less than a reasonable royalty or lost profits, together with pre-judgment and post-judgment interest and costs under 35 U.S.C. § 284;

c. award Whirlwind an accounting for acts of infringement not presented at trial and an award by the Court of additional damage for any such acts of infringement;

d. declare this case to be "exceptional" under 35 U.S.C. § 285 and award Whirlwind its attorneys' fees, expenses, and costs incurred in this action;

e. declare Defendant's infringement to be willful and treble the damages, including attorneys' fees, expenses, and costs incurred in this action and an increase in the damage award pursuant to 35 U.S.C. § 284;

f. a decree addressing future infringement that either (i) awards a permanent injunction enjoining Defendant and its agents, servants, employees, affiliates, divisions, and subsidiaries, and those in association with Defendant from infringing the claims of the Patents-in-Suit, or (ii) awards damages for future infringement in lieu of an injunction in an amount consistent with the fact that for future infringement the Defendant will be an adjudicated infringer of a valid patent, and trebles that amount in view of the fact that the future infringement will be willful as a matter of law; and

g. award Whirlwind such other and further relief as this Court deems just and proper.

DATED: November 30, 2021 Respectfully submitted,

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